Claim(s)

What is claimed is:

1. An interconnect system for conveying signals between first and second nodes within an electronic device and a third node external to said electronic device, the interconnect system comprising:

a first conductive path linking said first node to said third node; and

a second conductive path linking said second node to said third node, wherein said first and second conductive path are substantially inductive.

2. The interconnect system in accordance with claim 1 wherein said electronic device is an integrated circuit,

wherein said first and second nodes are bond pads implemented on said integrated circuit,

wherein said first conductive path comprises a first bond wire,

wherein said second conductive path comprises a second bond wire.

3. The interconnect system in accordance with claim 2 wherein inductances of said first and second bond wires are sized to substantially optimize a frequency response characteristic of said interconnect system.

4. The interconnect system in accordance with claim 2 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductances of said first and second bond wires are sized to substantially optimize a frequency response characteristic of said interconnect system.

5. The interconnect system in accordance with claim 2 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductance of said first and second bond wires are sized so that the interconnect system has a frequency response

substantially similar to a frequency response of a Butterworth filter.

6. The interconnect system in accordance with claim 2 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductance of said first and second bond wires are sized so that the interconnect system has a frequency response substantially similar to a frequency response of a Chebyshev filter.

7. The interconnect system in accordance with claim 1 wherein inductances of said first and second conductive paths are sized to substantially optimize a frequency response characteristic of said interconnect system.

8. The interconnect system in accordance with claim 1 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductances of said first and second conductive paths are sized to substantially optimize a frequency response characteristic of said interconnect system.

9. The interconnect system in accordance with claim 1 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductances of said first and second conductive paths are sized so that the interconnect system has a frequency response substantially similar to a frequency response of a Butterworth filter.

10. The interconnect system in accordance with claim 1 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductances of said first and second conductive paths are sized so that the interconnect system has a frequency response substantially similar to a frequency response of a Chebyshev filter.

11. The interconnect system in accordance with claim 10 wherein said third node comprises a trace on a printed circuit board, and

wherein said capacitive element comprises a via in said printed circuit board, said via being connected to said trace.

12. The interconnect system in accordance with claim 1 wherein said electronic device is an integrated circuit, and

wherein said first and second conductive paths are implemented by a spring contact comprising:

a tip for contacting said third node,

a first conductive leg connected between said first node and said tip, and

a second conductive leg connected between said second node and said tip.

13. The interconnect system in accordance with claim 12 wherein inductances of each of said first and second conductive legs are sized to substantially optimize a frequency response characteristic of said interconnect system.

14. The interconnect system in accordance with claim 12 further comprising a capacitive element linked to said third node, wherein capacitance of said capacitive element and inductances of said first and second conductive legs are sized to substantially optimize a frequency response characteristic of said interconnect system.

15. The interconnect system in accordance with claim 14 wherein said third node comprises a contact point on a printed circuit board trace for receiving said tip and wherein said capacitive element comprises a printed circuit board via connected to said printed circuit board trace.

16. The interconnect system in accordance with claim 12 wherein said conductive legs comprise resilient material.

17. The interconnect system in accordance with claim 12 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductance of said first and second conductive legs are sized so that the interconnect system has a frequency response substantially similar to a frequency response of a Butterworth filter.

18. The interconnect system in accordance with claim 12 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element and inductance of said first and second conductive legs are sized so that the interconnect system has a frequency response substantially similar to a frequency response of a Chebyshev filter.

19. An interconnect system for conveying signals between first and second nodes internal to an integrated circuit and a third node external to the integrated circuit, the interconnect system comprising:

an inductor connected between said first node and said second node, and

a conductor connected between said second node and said third node.

20. The interconnect system in accordance with claim 19

wherein said first node comprises a first bond pad implemented on said integrated circuit,

wherein said second node comprises a second bond pad implemented on said integrated circuit, and

wherein said inductor consists of a bond wire connected between said first and second bond pads.

21. The interconnect system in accordance with claim 19 wherein said inductor is implemented within said integrated circuit.

22. The interconnect system in accordance with claim 21 wherein said inductor comprises a lithographically defined conductive trace.

23. The interconnect system in accordance with claim 19 further comprising a capacitive element connected to said third node, wherein capacitance of said capacitive element is sized to substantially optimize a frequency response characteristic of said interconnect system.

24. The interconnect system in accordance with claim 23,

wherein said third node comprises a printed circuit board trace, and

wherein said capacitive element comprises a printed circuit board via connected to said printed circuit board trace.

25. The interconnect system in accordance with claim 19 wherein the interconnect system has a frequency response substantially similar to that of a Butterworth filter.

26. The interconnect system in accordance with claim 19 wherein the interconnect system has a frequency response substantially similar to that of a Chebyshev filter.